

FIG. 1

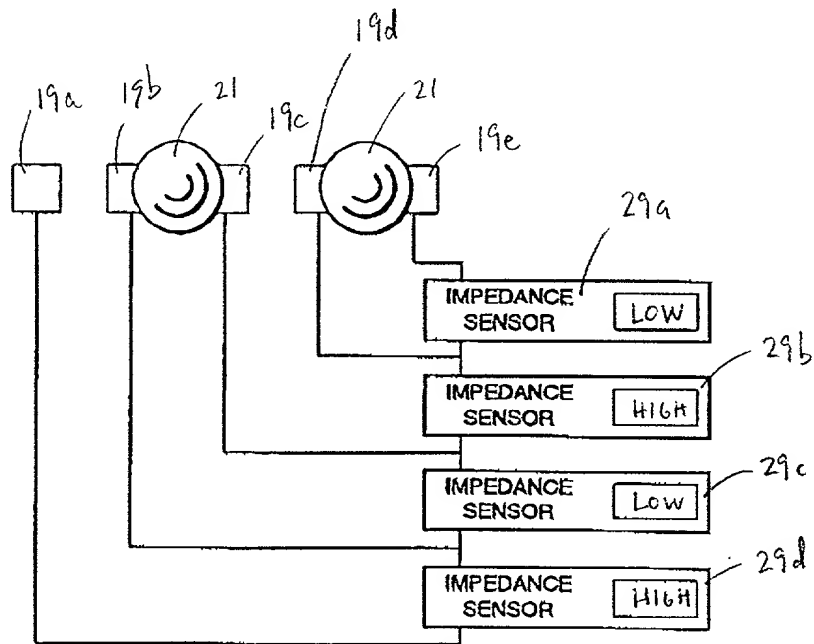


FIG. 3

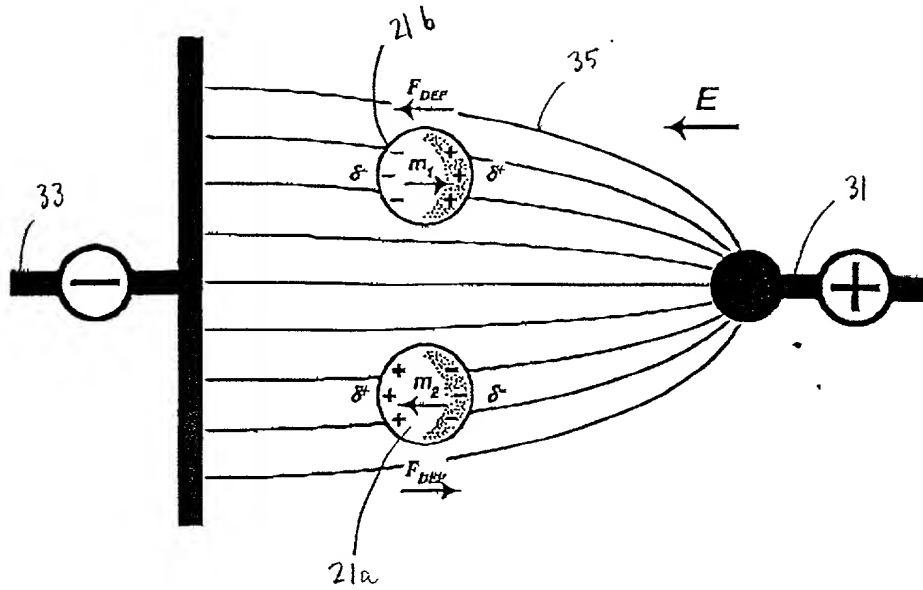


FIG. 2

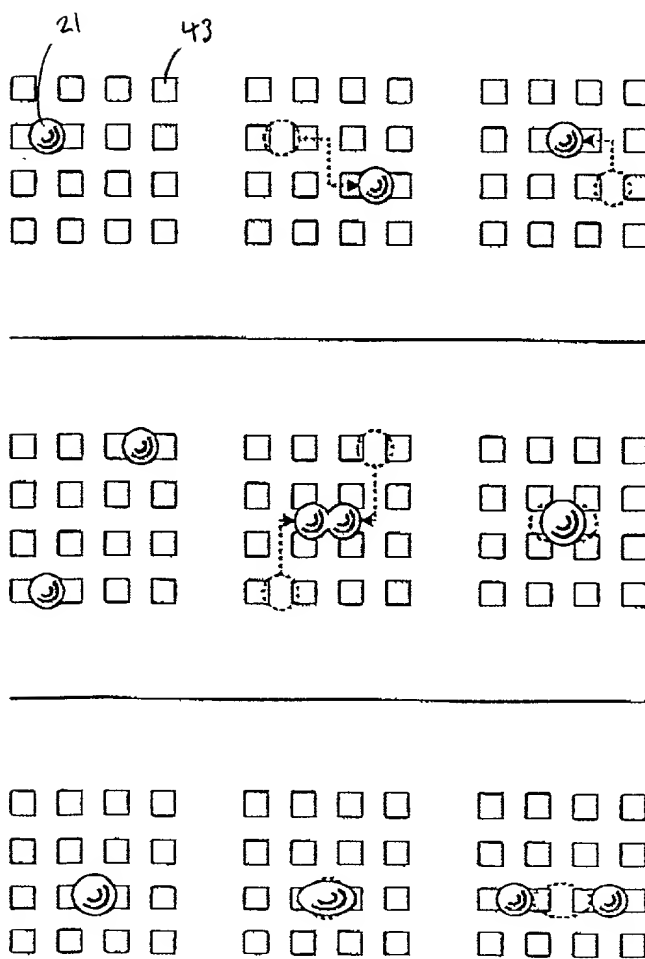


FIG. 12

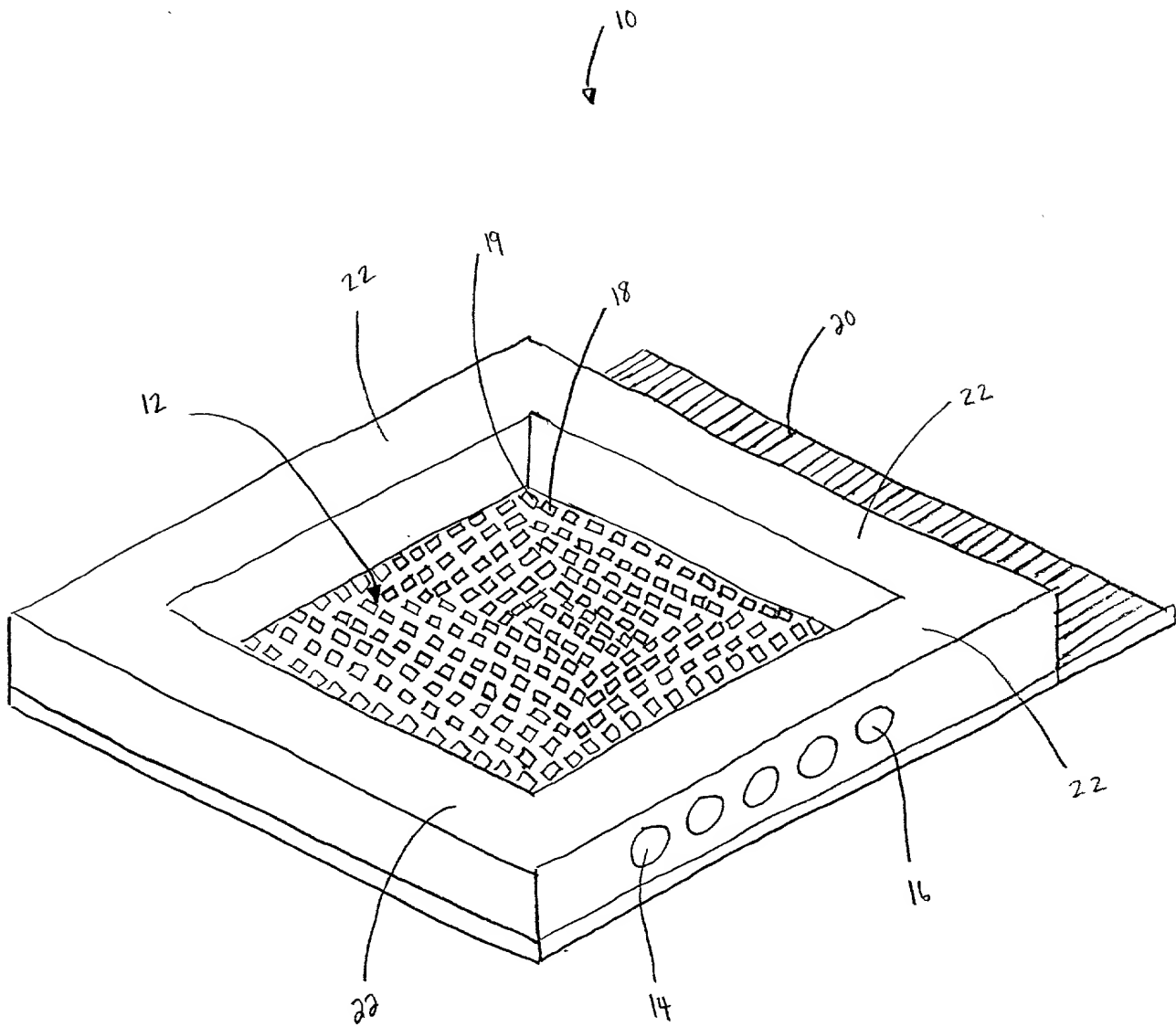


FIG. 4

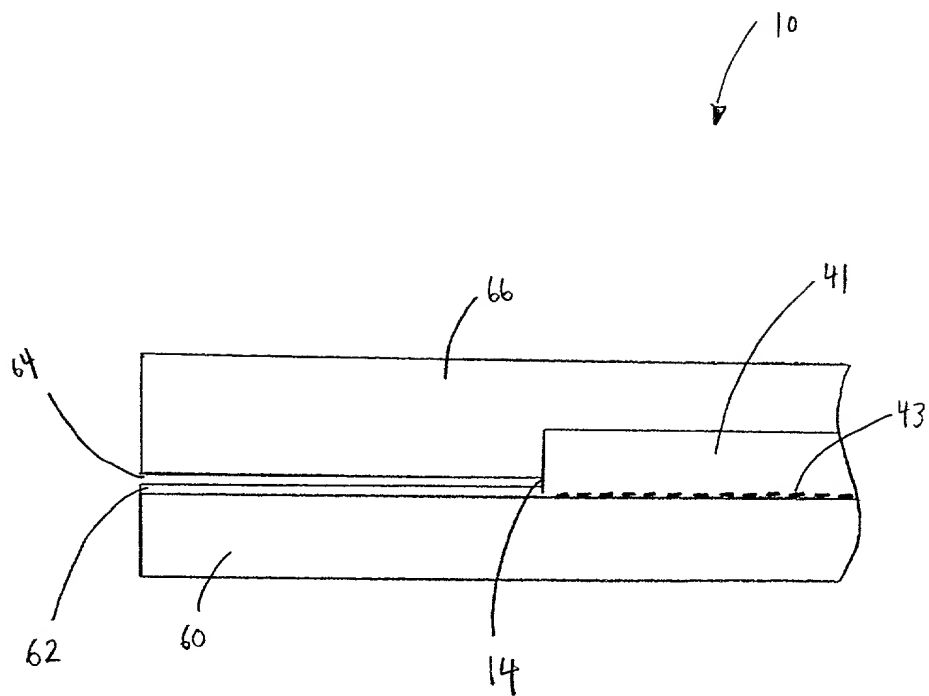


FIG. 5

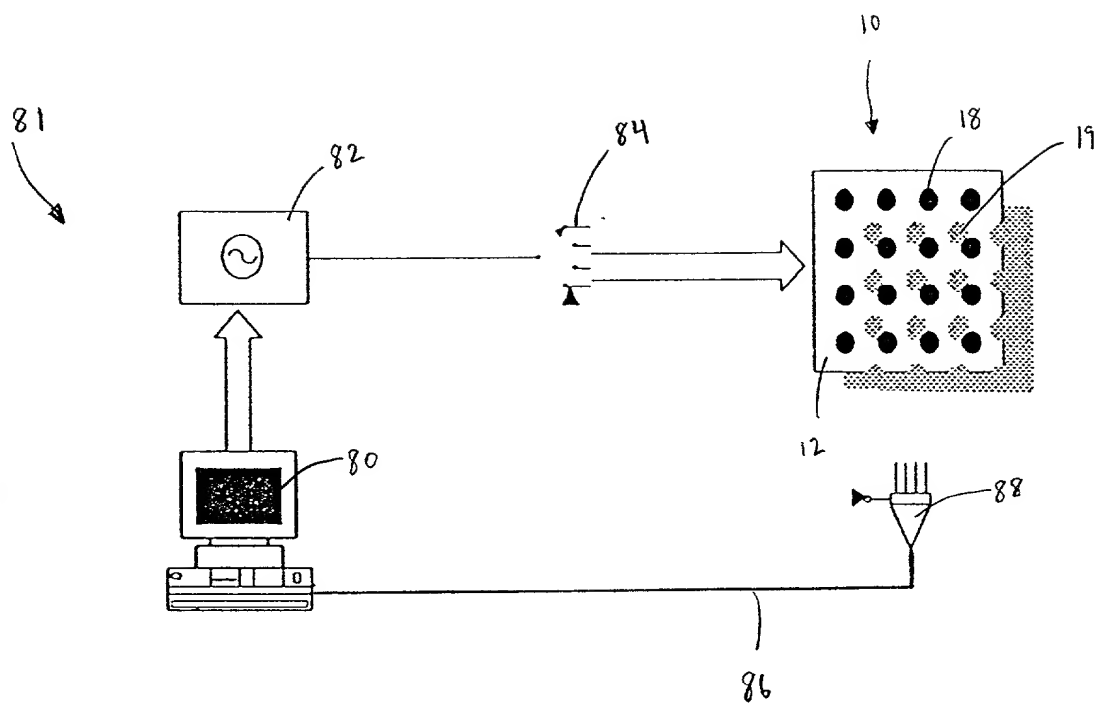


FIG. 6

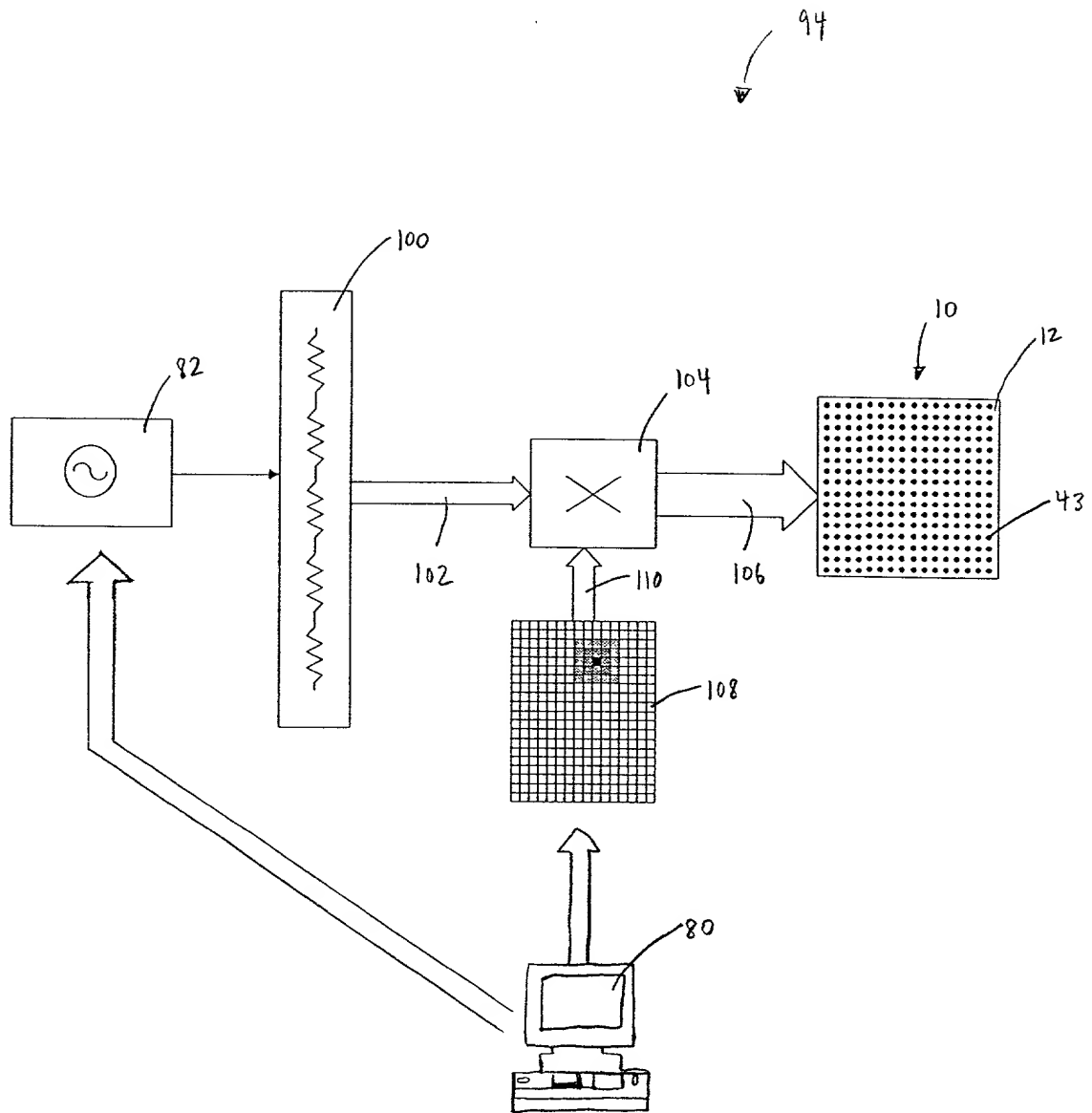


FIG. 7

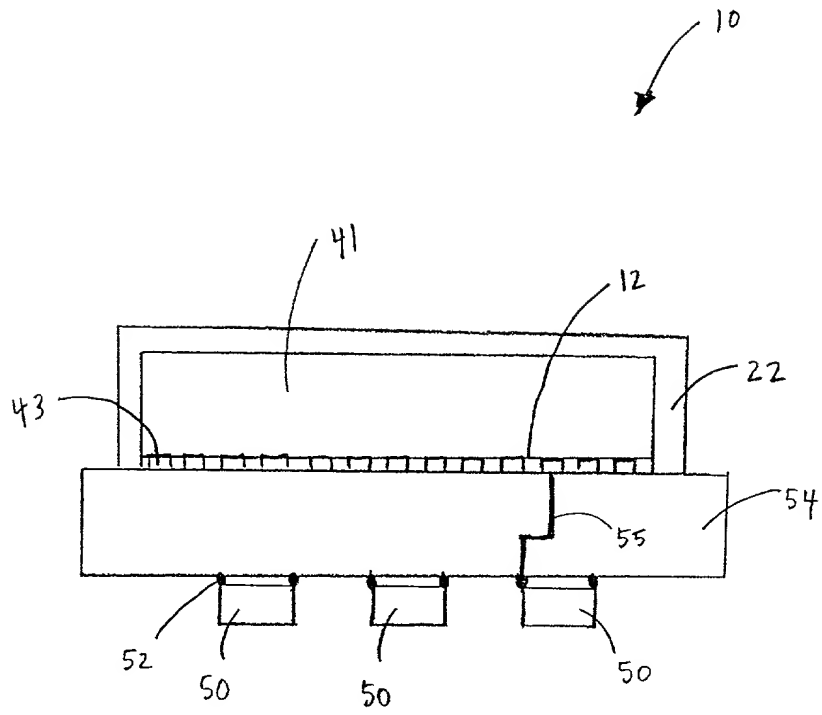


FIG. 8

FIG. 9

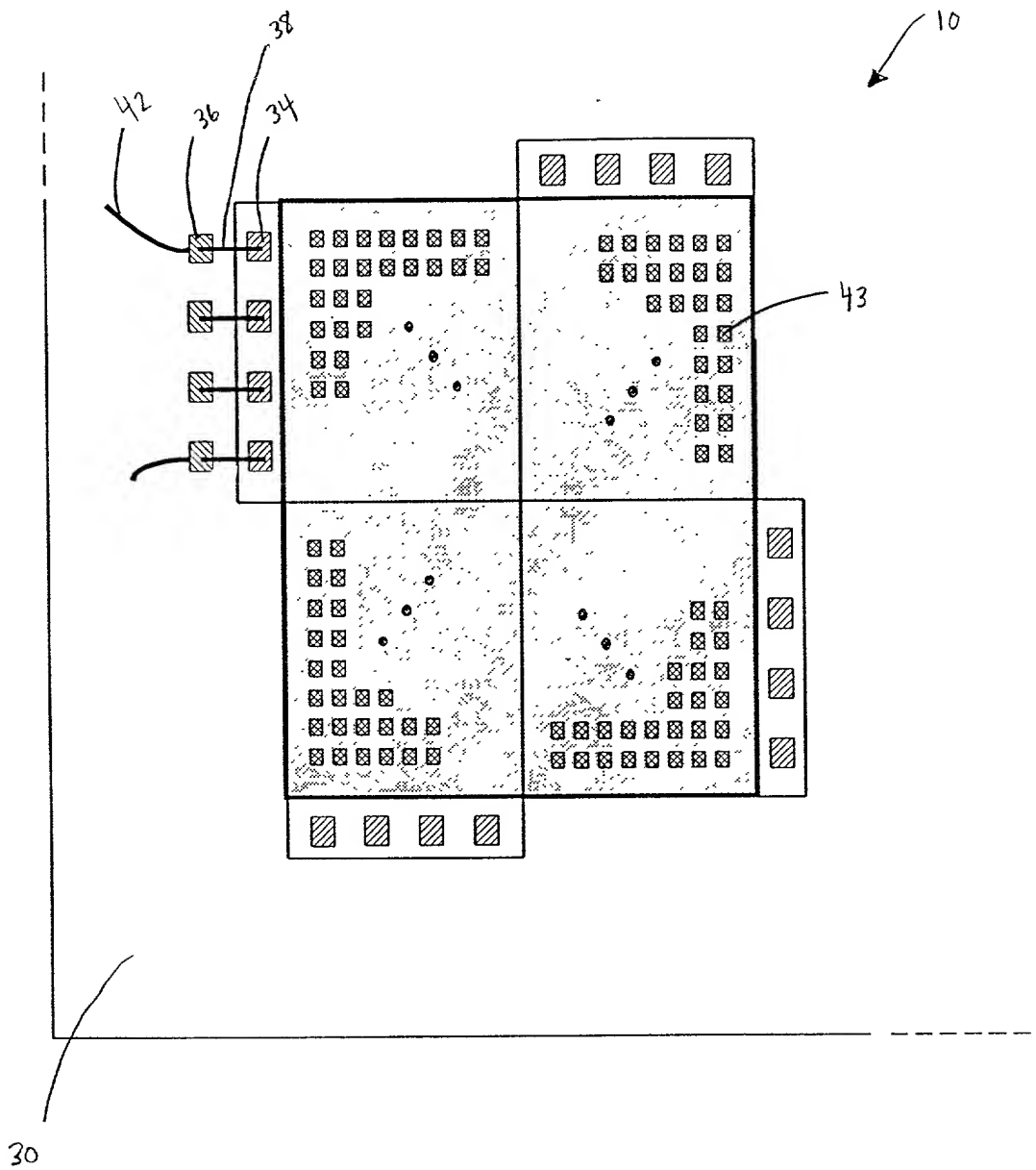


FIG. 9

Multiple programmable inlet/outlet
ports along edges of processor

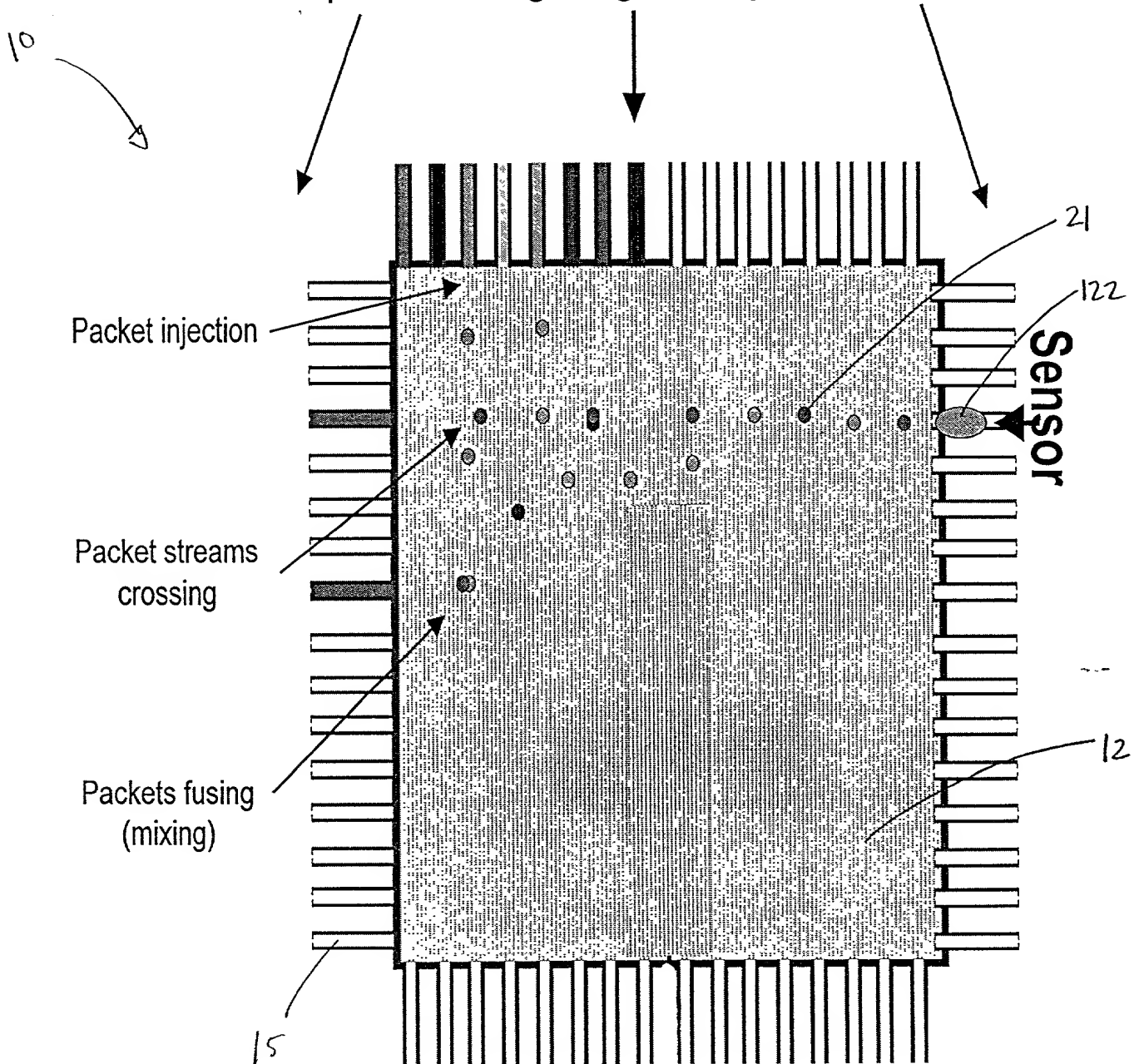


FIG. 9B

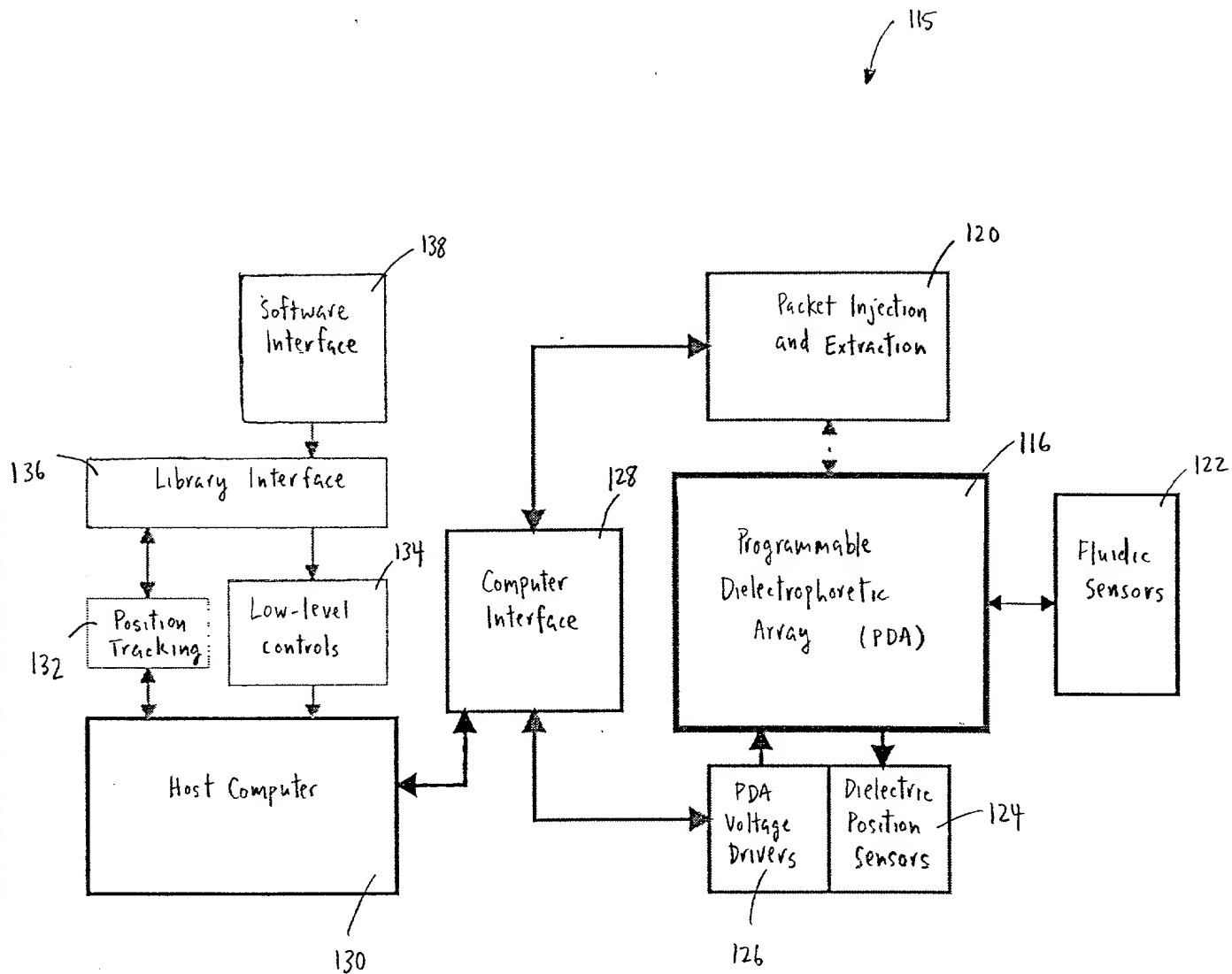


FIG. 10

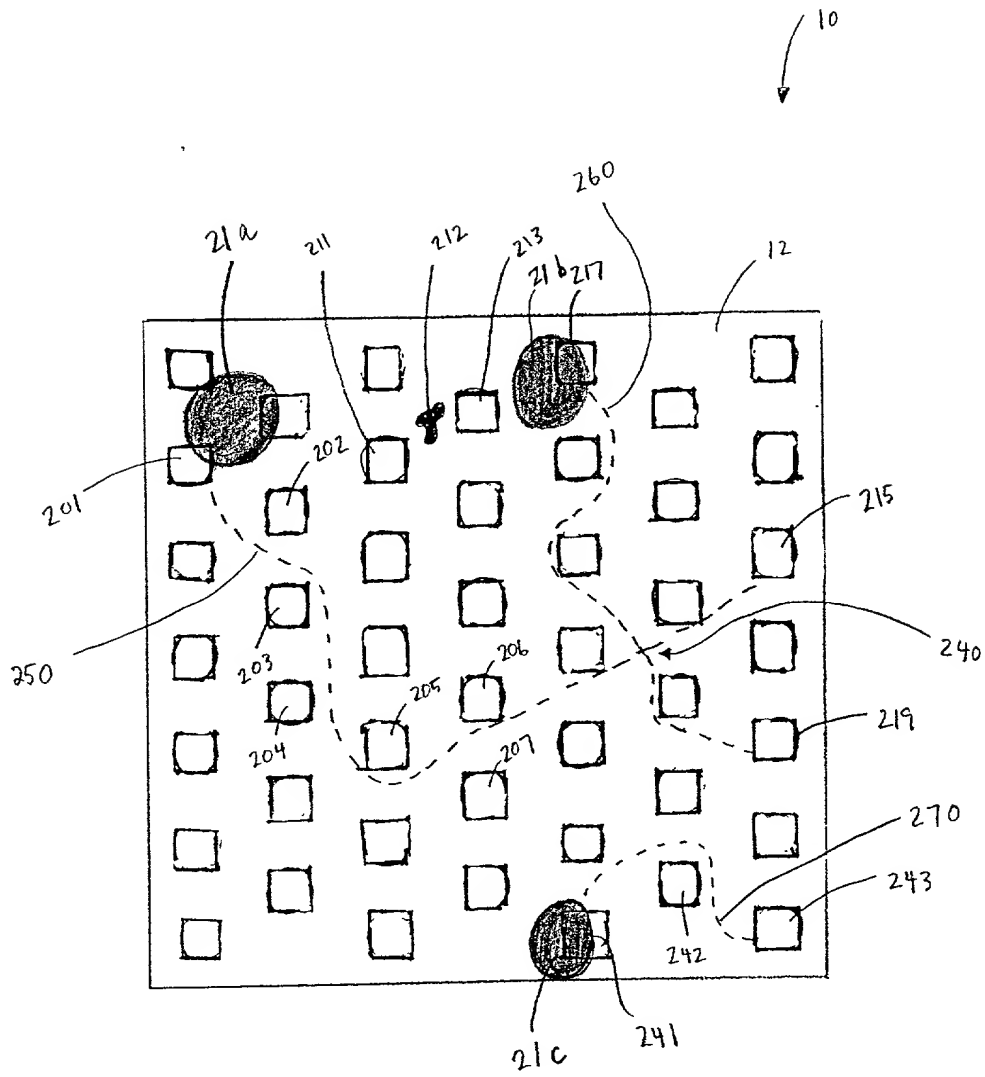


FIG. 11

